ABSTRACT

A high-speed digital multiplexer is disclosed. The multiplexer includes a plurality of input pins for receiving a plurality of digital input signals and switching circuitry coupled to the input pins. The switching circuitry has respective outputs coupled to a common node and is operative to enable a selected one of the plurality of input pins. The multiplexer further includes a local signal converter having a circuit branch set to a common voltage. The branch is connected to the common node to sense changes in current corresponding to an input signal received by an enabled input pin. An output pin is coupled to the local signal converter, whereby the local signal converter is operative to produce voltage changes at the output corresponding to the sensed current changes.